09/591615

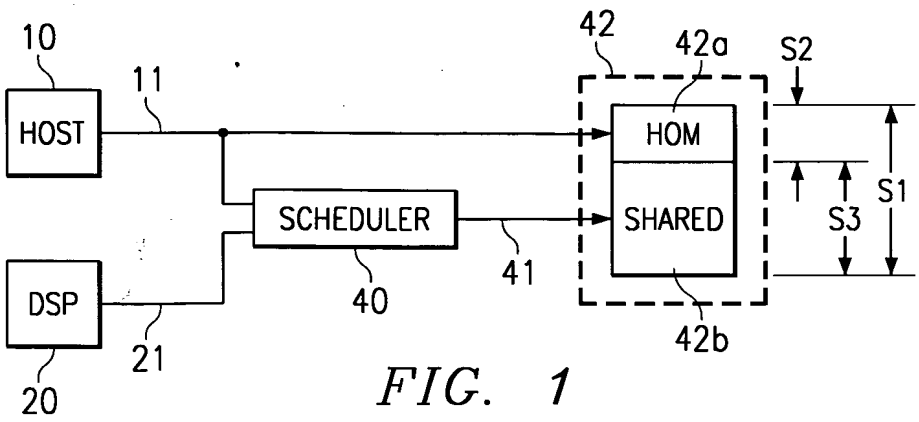


FIG. 1

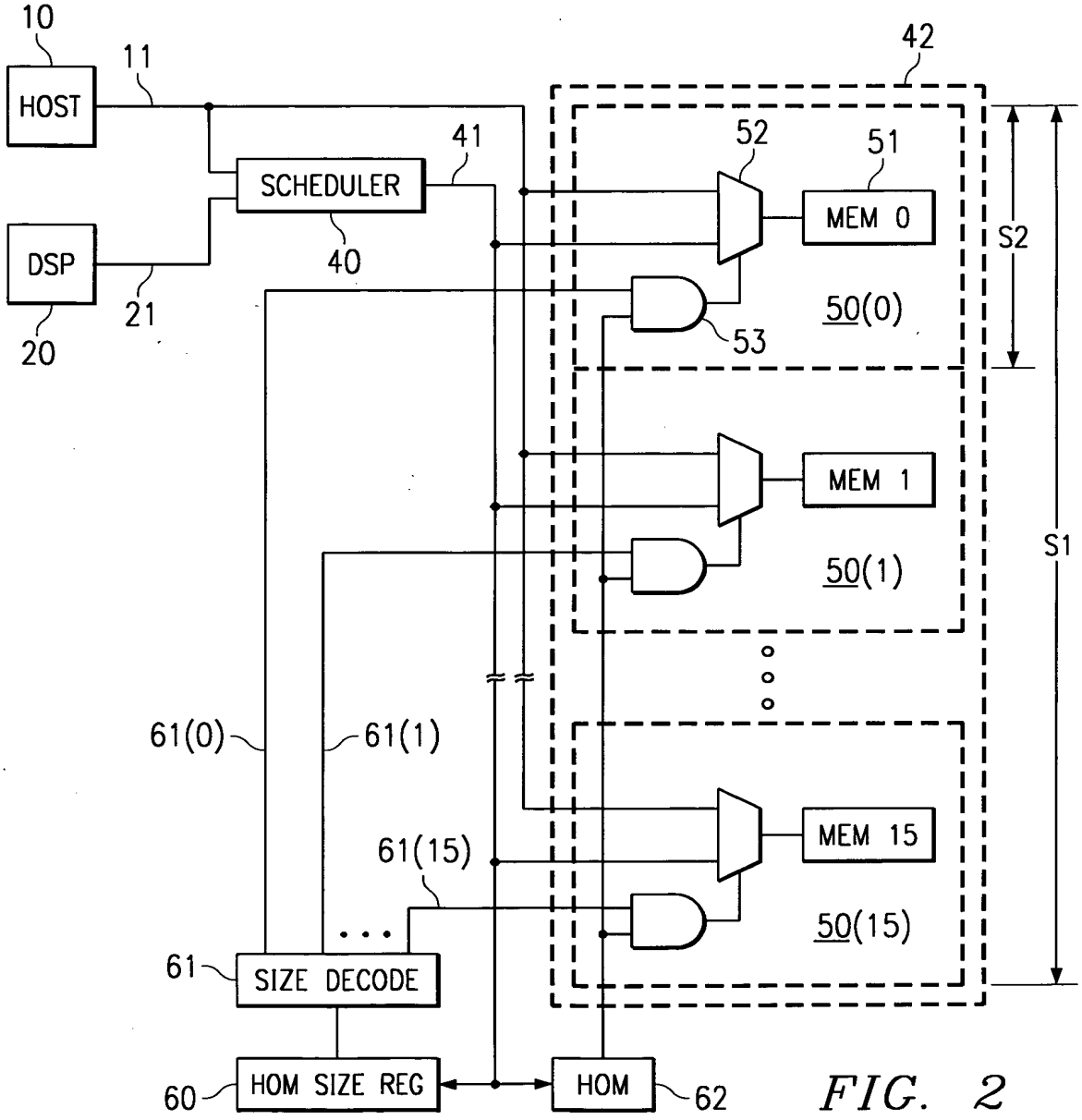


FIG. 2

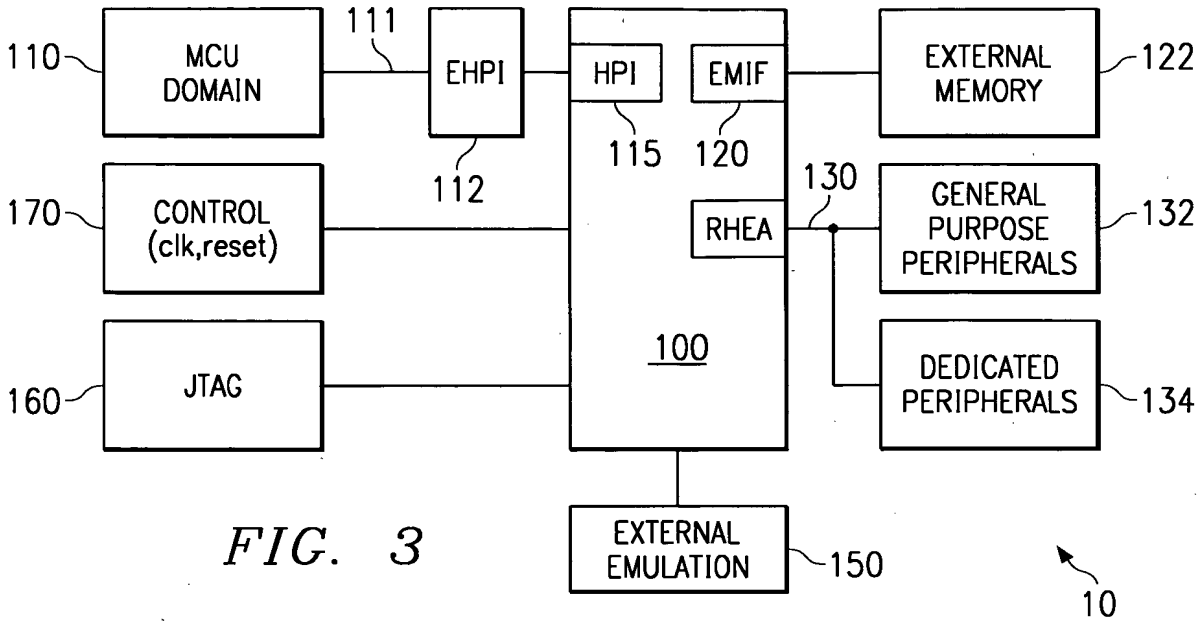

110
MCU DOMAIN
111
EHPI
112
HPI
115
EMIF
120
EXTERNAL MEMORY
122
170
CONTROL (clk,reset)
RHEA
130
GENERAL PURPOSE PERIPHERALS
132
100
160
JTAG
DEDICATED PERIPHERALS
134
EXTERNAL EMULATION
150
10

FIG. 3

FIG. 4

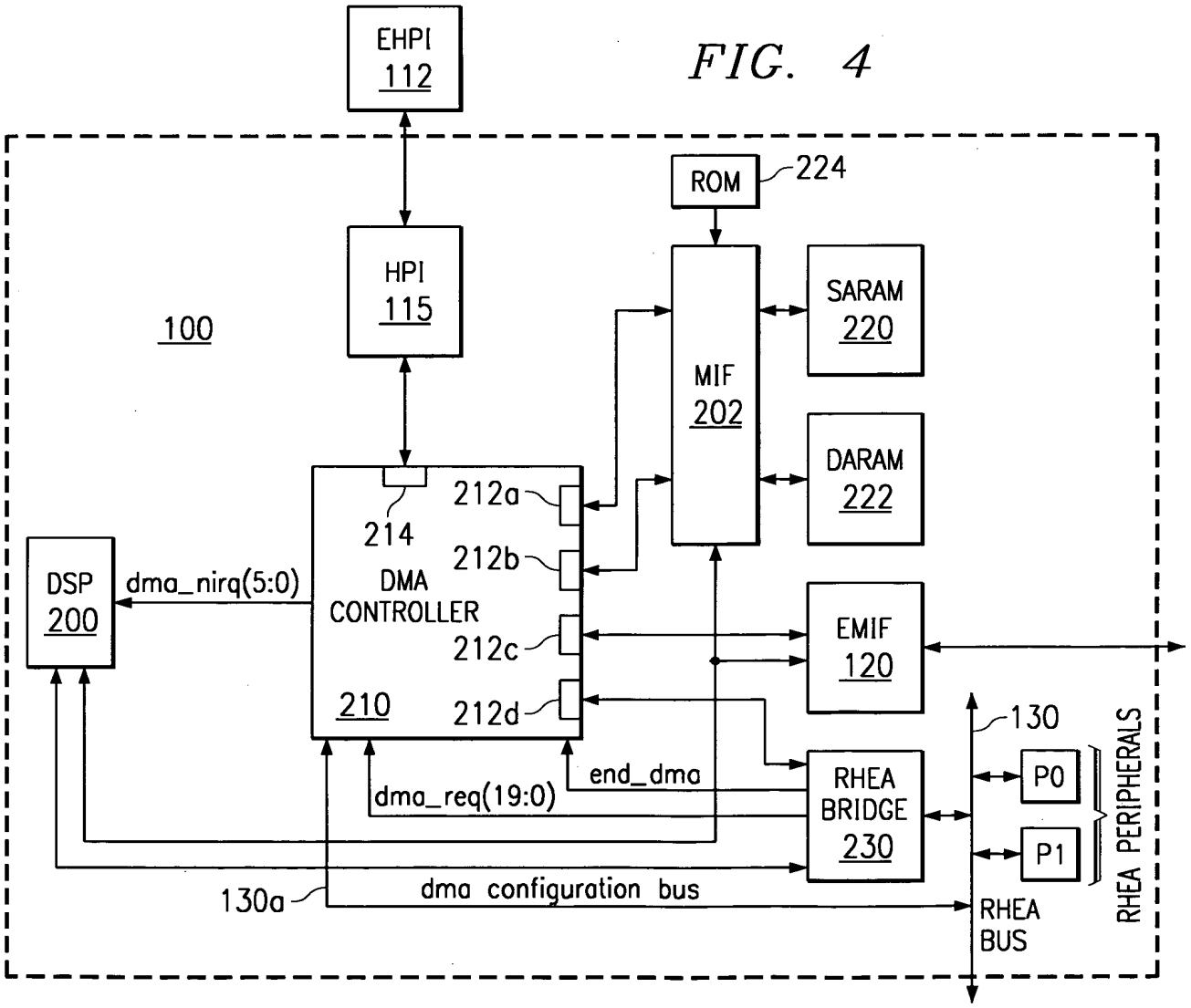
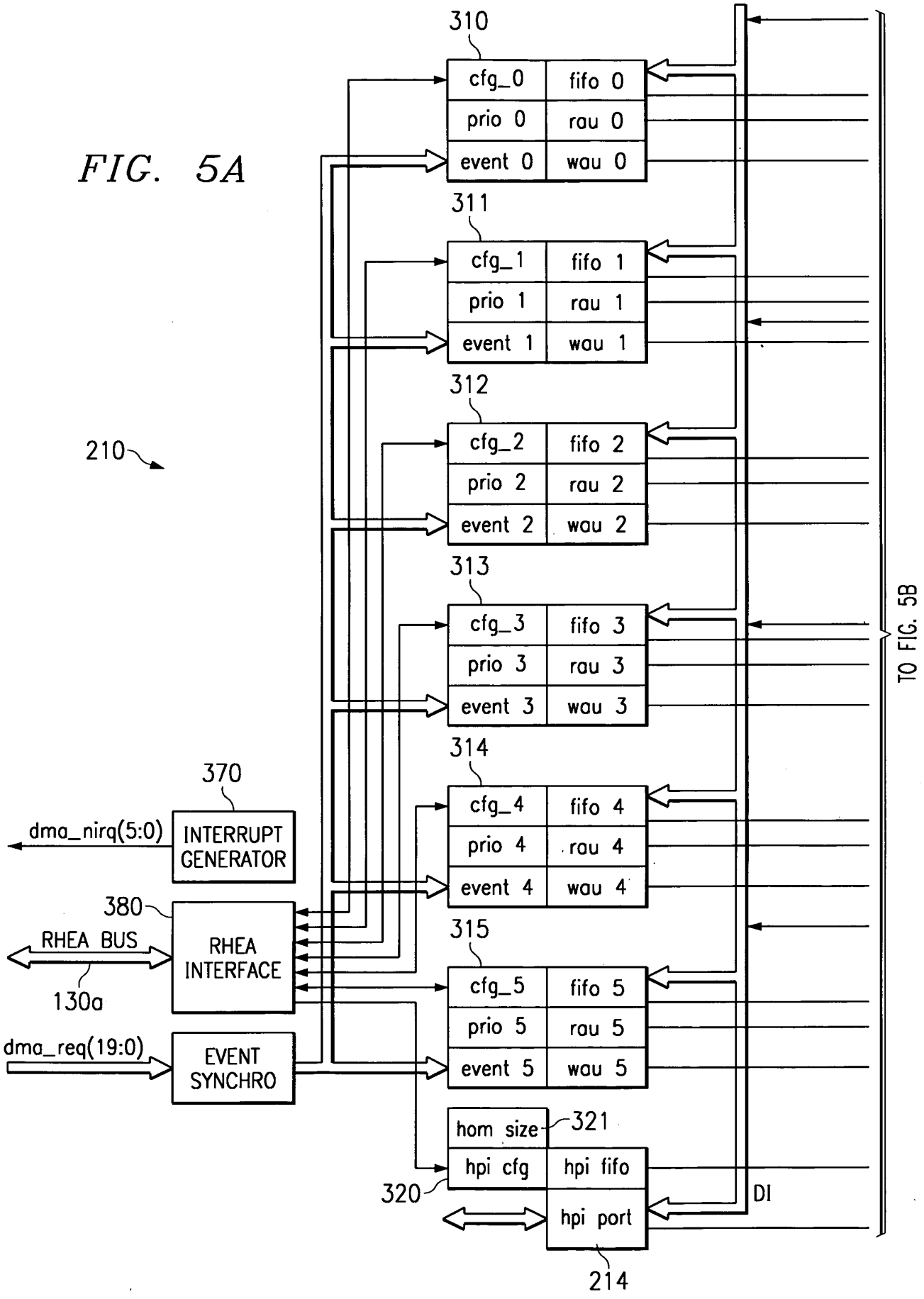

EHPI
112
ROM
224
HPI
115
100
SARAM
220
MIF
202
DARAM
222
214
212a
212b
DSP
200
dma_nirq(5:0)
DMA CONTROLLER
212c
EMIF
120
210
212d
130
end_dma
dma_req(19:0)
RHEA BRIDGE
230
P0
P1
RHEA PERIPHERALS
130a
dma configuration bus
RHEA BUS

FIG. 5A


210
310
cfg_0
fifo 0
prio 0
rau 0
event 0
wau 0
311
cfg_1
fifo 1
prio 1
rau 1
event 1
wau 1
312
cfg_2
fifo 2
prio 2
rau 2
event 2
wau 2
313
cfg_3
fifo 3
prio 3
rau 3
event 3
wau 3
314
cfg_4
fifo 4
prio 4
rau 4
event 4
wau 4
315
cfg_5
fifo 5
prio 5
rau 5
event 5
wau 5
370
INTERRUPT GENERATOR
dma_nirq(5:0)
380
RHEA INTERFACE
RHEA BUS
130a
EVENT SYNCHRO
dma_req(19:0)
hom size
321
hpi cfg
hpi fifo
320
hpi port
214
DI
TO FIG. 5B

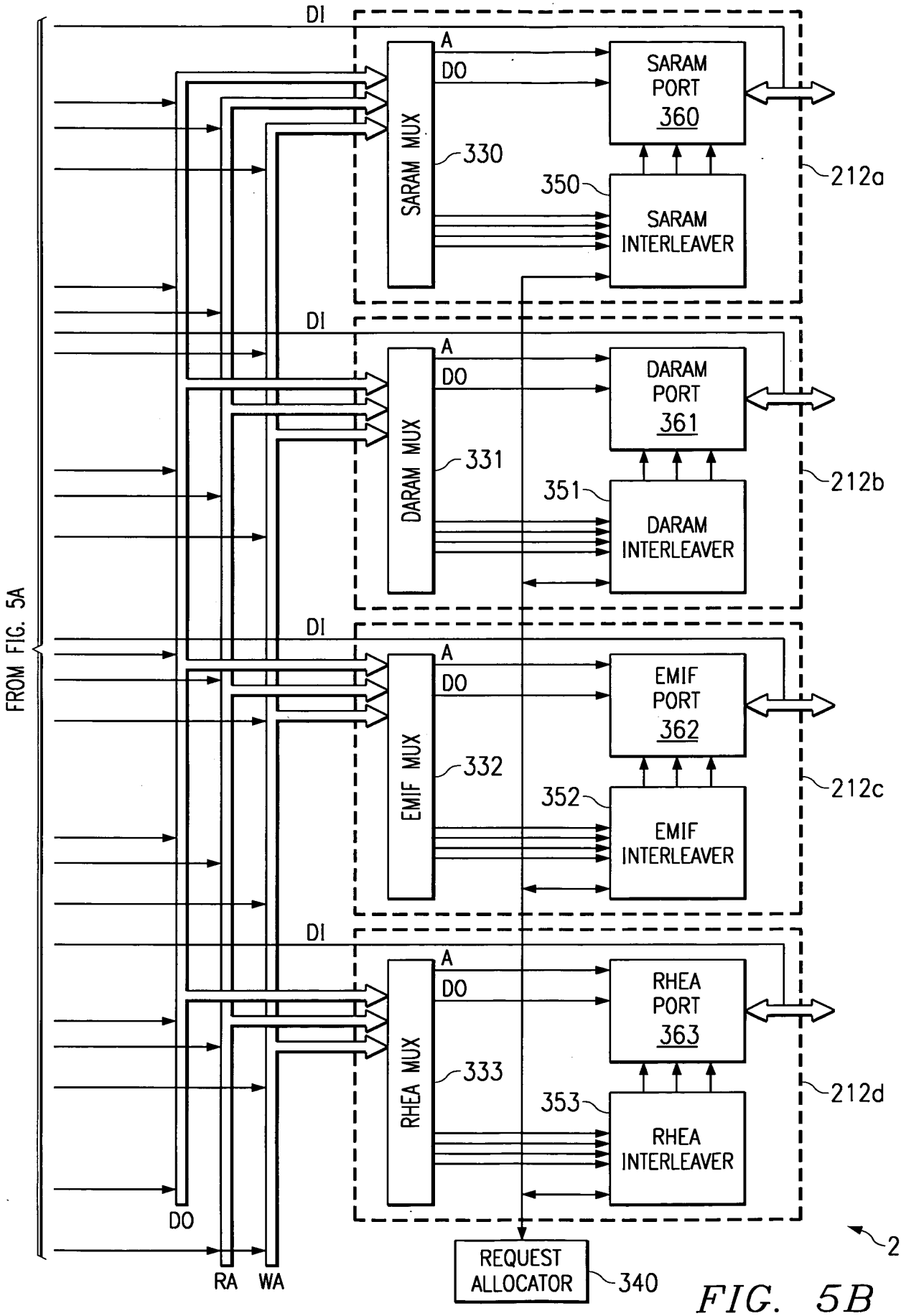

FROM FIG. 5A
DI
A
DO
SARAM MUX
330
SARAM PORT
360
350
SARAM INTERLEAVER
212a
DARAM MUX
331
DARAM PORT
361
351
DARAM INTERLEAVER
212b
EMIF MUX
332
EMIF PORT
362
352
EMIF INTERLEAVER
212c
RHEA MUX
333
RHEA PORT
363
353
RHEA INTERLEAVER
212d
RA
WA
REQUEST ALLOCATOR
340
210

FIG. 5B

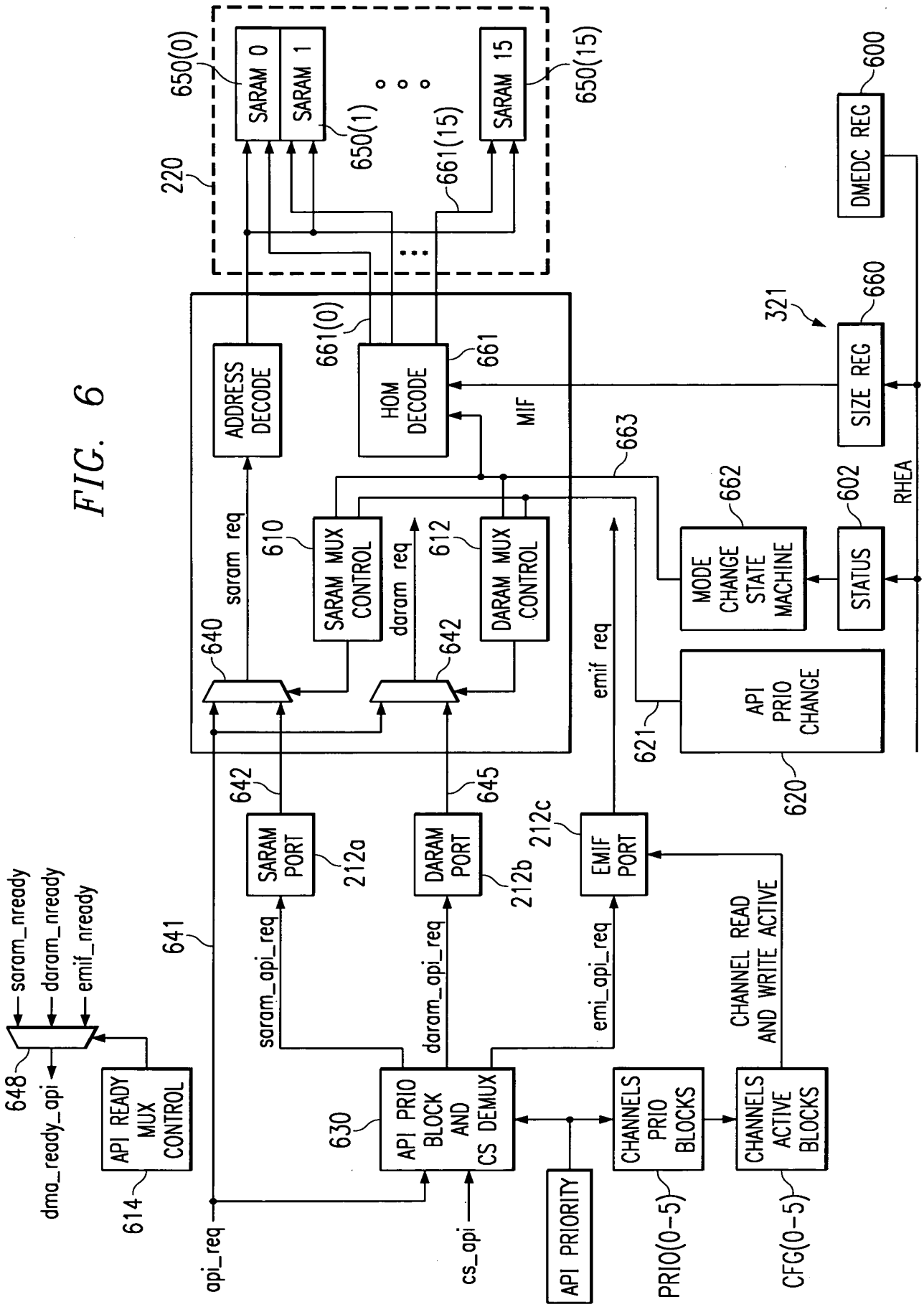

650(0)
SARAM 0
SARAM 1
650(1)
SARAM 15
650(15)
220
661(15)
661(0)
661
ADDRESS DECODE
HOM DECODE
MIF
DMEDC REG
600
321
660
SIZE REG
RHEA
602
STATUS
662
MODE CHANGE STATE MACHINE
663
saram req
610
SARAM MUX CONTROL
daram req
612
DARAM MUX CONTROL
640
642
emif req
API PRIO CHANGE
621
620
642
645
212c
SARAM PORT
212a
DARAM PORT
212b
EMIF PORT
641
saram_nready
daram_nready
emif_nready
saram_api_req
daram_api_req
emi_api_req
CHANNEL READ AND WRITE ACTIVE
648
dma_ready_api
API READY MUX CONTROL
614
630
API PRIO BLOCK AND CS DEMUX
CHANNELS PRIO BLOCKS
CHANNELS ACTIVE BLOCKS
api_req
cs_api
API PRIORITY
PRIO(0-5)
CFG(0-5)

FIG. 6

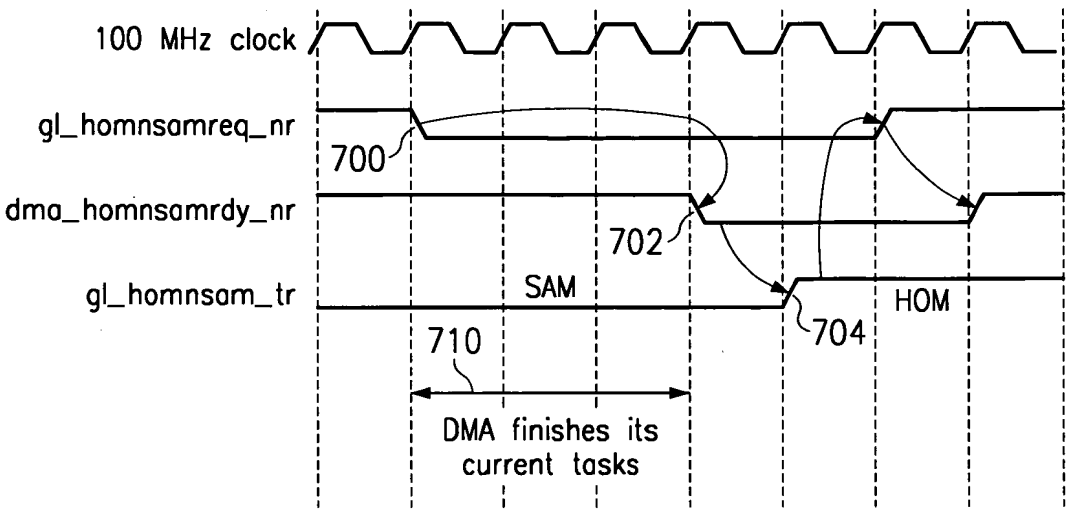

100 MHz clock
gl_homnsamreq_nr
700
dma_homnsamrdy_nr
702
gl_homnsam_tr
SAM
HOM
704
710
DMA finishes its
current tasks

FIG. 7A

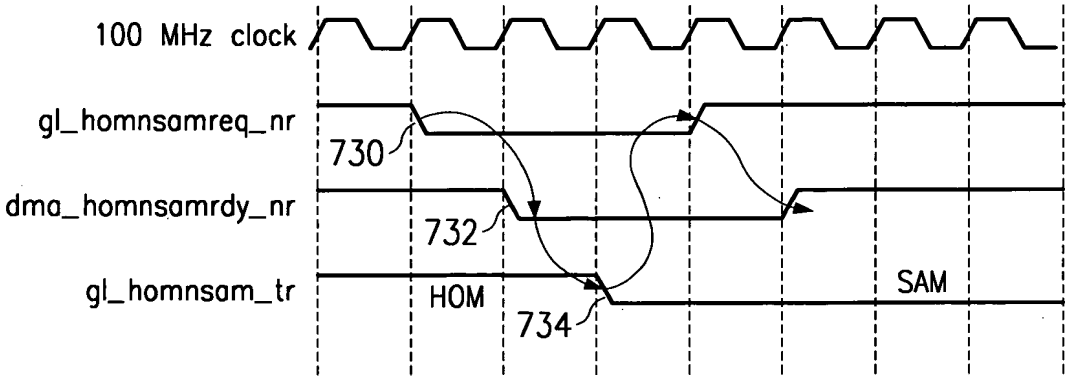

100 MHz clock
gl_homnsamreq_nr
730
dma_homnsamrdy_nr
732
gl_homnsam_tr
HOM
734
SAM

FIG. 7B

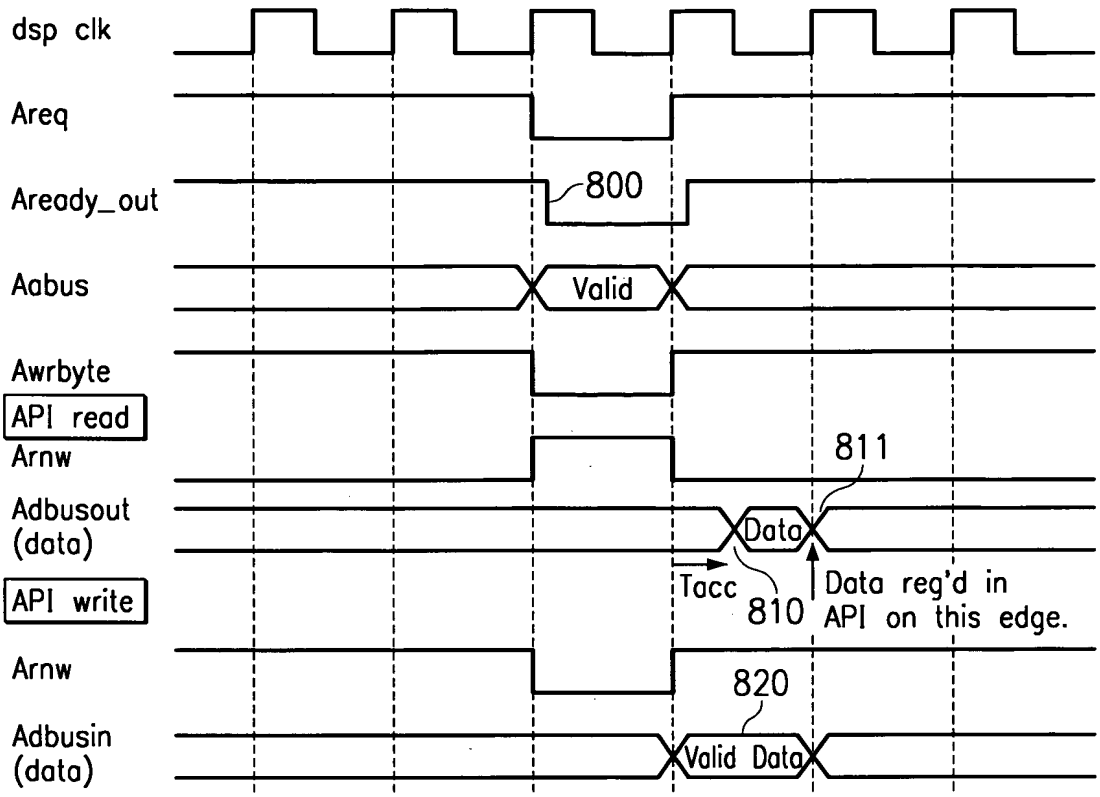

dsp clk
Areq
Aready_out
800
Aabus
Valid
Awrbyte
API read
Arnw
811
Adbusout
(data)
Data
Tacc
810
Data reg'd in
API on this edge.
API write
Arnw
820
Adbusin
(data)
Valid Data

FIG. 8

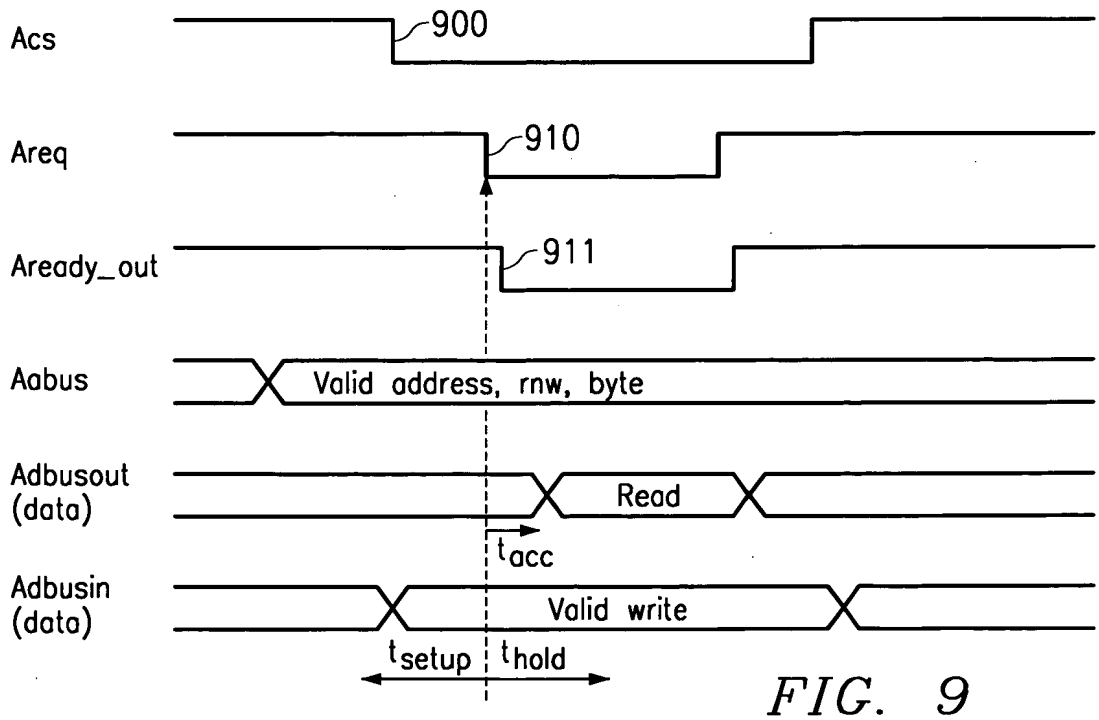

Acs
900
Areq
910
Aready_out
911
Aabus
Valid address, rnw, byte
Adbusout
(data)
Read
tacc
Adbusin
(data)
Valid write
tsetup
thold

FIG. 9

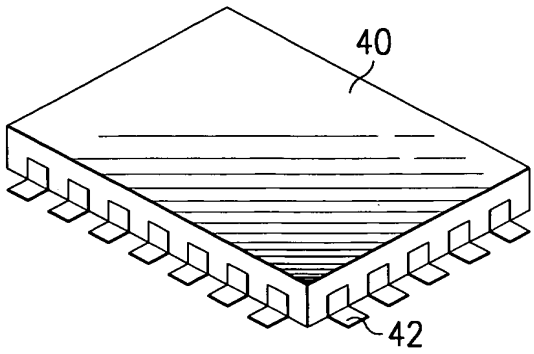


FIG. 10

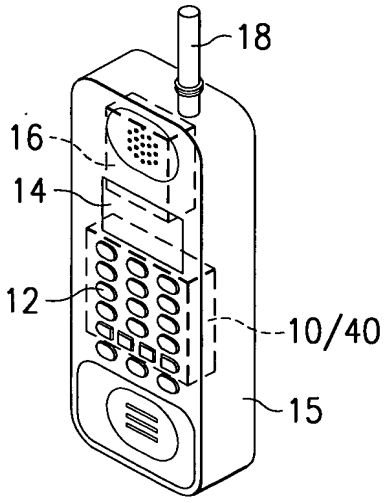


FIG. 11